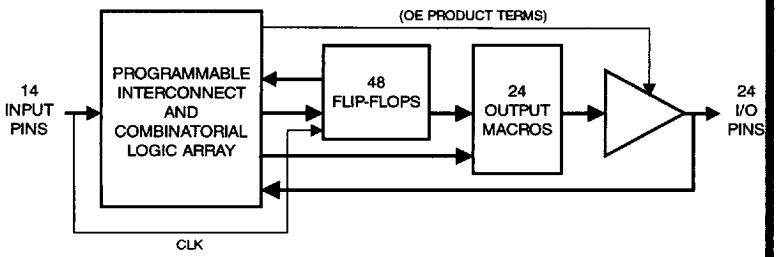
Features

- 3-Volt Operation
- Wide V_{CC} Range
  - V_{CC} = 3.0 V to 5.25 V (Commercial)
  - V_{CC} = 3.0 V to 5.5 V (Industrial)
- High Performance, High Density Programmable Logic Device
  - Maximum 15 ns Pin-to-Pin Delay
  - Fully Connected Logic Array With 416 Product Terms
- Flexible Output Macrocell
  - 48 Flip-Flops - Two per Macrocell
  - 72 Sum Terms
  - All Flip-Flops, I/O Pins Feed In Independently
  - Achieves Over 80% Gate Utilization
- Enhanced Macrocell Configuration Selections
  - D- or T-Type Flip-Flops
  - Product Term or Direct Input Pin Clocking
  - Registered or Combinatorial Internal Feedback
- Low Power ATLV2500BL - 7.2 mW Stand-By (Typical) at 3.6 V
- Backward Compatible With ATV2500H/L Software
- Proven and Reliable High Speed UV EPROM Process
- Reprogrammable - Tested 100% for Programmability
- 44-Lead Surface Mount Packages

High Speed High Density UV Erasable Programmable Logic Device

Advance Information

Block Diagram



Description

The ATLV2500Bs are the highest density PLDs available in a 44-pin package. With their fully connected logic array and flexible macrocell structure, high gate utilization is easily obtainable.

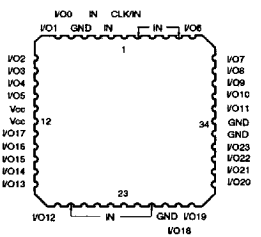
The ATLV2500Bs are organized around a *single universal input bus*. All pin and feedback terms are always available to every macrocell. Each of the 38 logic pins are array inputs, as are the outputs of each flip-flop.

(continued)

Pin Configurations

Pin Name	Function
IN	Logic Inputs
CLK/IN	Pin Clock and Input
I/O	Bidirectional Buffers
GND	Ground
Vcc	+5 V Supply

SMD



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Description (Continued)

In the ATLV2500Bs, four product terms are input to each sum term. Furthermore, each macrocell's three sum terms can be combined to provide up to 12 product terms per sum term with *no performance penalty*. Each flip-flop is individually selectable to be either D- or T-type, providing further logic compaction. Also, 24 of the flip-flops may be bypassed to provide internal combinatorial feedback to the logic array.

Product terms provide individual clocks and asynchronous resets for each flip-flop. The flip-flops may also be individually configured to have direct input pin clocking. Each output has its own enable product term. Eight synchronous preset product terms serve local groups of either four or eight flip-flops. Register preload functions are provided to simplify testing. All registers automatically reset upon power up.

The ATLV2500BL is the low voltage compatible device with speeds as fast as 20 ns. The ATLV2500BL consumes only 2 mA at standby, which provides the optimum low power PLD solution with full CMOS output levels. The ATLV2500BL significantly reduces total system power, allowing battery-powered operation.

D.C. and A.C. Operating Conditions

	Commercial -15, -20	Industrial -15, -20
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	3.0 V to 5.25 V	3.0 V to 5.5 V